in revised drawings attached hereto. The revised drawings show the proposed changes in red, which are submitted for approval by the Examiner. Upon approval of the revised drawings, the Applicant will submit new drawings in compliance with 37 C.F.R. § 1.84 including the changes.

II. Discussion of Rejection of Claims 1-10 Under 35 U.S.C. § 103(a)

In paragraph 3 of the Office Action, the Examiner rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,150,280 to Arai, et al.

In rejecting Claims 1-10, the Examiner stated that "Arai teaches a silicon platform for optical modules" in reference to elements 20 and 16 of Figure 1 of Arai. The Examiner further stated that the electronic circuit package of Arai's Figure 18 comprises "a silicon substrate" as element 16, and "a first insulating layer formed on the silicon substrate" as element 120. The Examiner described Arai's electronic circuit package as comprising "a first conductor layer formed on the first insulating layer ... ; a second insulating layer formed on the first conductive layer ... ; and a conductor layer formed on the second insulating layer" in reference to column 14, lines 42-54 of Arai. On page 3 of the Office Action, the Examiner asserted that "Arai further teaches conductor layer overlying the first insulating layer" in reference to the insulator 50 and ground pattern 58 of Arai's Figure 18. The Examiner acknowledged that "Arai does not explicitly state that" the "conductor layer" is "the end portion of the second conductor layer." However, the Examiner argued that it would have been "obvious to a person of ordinary skill in the art that first conducting/ground layer overlying ... the chip/silicon substrate is an end portion of the second or third conducting layer 58/62 through the extended ground strips 64 that connects these conducting/ground layers together provided that the chip/silicon substrate layer is the first insulation layer".

Arai general discloses an electronic circuit package wherein grounding is strengthened to restrain deterioration of a high speed characteristic of the package and a process of producing such electronic circuit package. *Arai at col. 3, lines 2-7.* In its Figure 18, Arai describes a receiving table 120 as composed of a plurality of dielectric layers and conductor layers layered in an alternate relationship to each other. *Id. at col. 14, lines 52-54.* The receiving table 120 is positioned between an IC chip 24 and a metal member 16, which denotes a second metal member

made of CuW and having spaces to each of which the IC chip 24 is to be secured. *Id. at col. 7, lines 45-47 and col. 14, lines 42-52; Fig. 18.*

It is well-settled that to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 U.S.P.Q. 580. The Applicant respectfully submits that Arai does not teach or suggest all of the claim limitations of Claim 1.

Claim 1 recites a silicon platform for optical modules, comprising "a silicon substrate; a first insulating layer formed on the silicon substrate; a first conductor layer formed on the first insulating layer; a second insulating layer formed on the first conductor layer; and a second conductor layer formed on the second insulating layer, an end portion of the second conductor layer overlying the first insulating layer to constitute bonding portions connected to lead wires." As discussed below, nowhere does Arai teach or suggest all the elements of Claim 1.

The Examiner refers to Arai's element 16 as teaching a "silicon substrate". However, according to Arai the "reference numeral 16 denotes a second metal member made of CuW and having spaces to each of which an IC chip is to be secured." *Col. 7, lines 45-47.* The only suggestion of a "silicon substrate" by Arai is in reference to the IC chip 26 of Figure 18, and a "metal member made of CuW" cannot be properly construed as teaching or suggesting the metal member is a silicon substrate. Therefore, Applicant responds herein under the assumption the Examiner intended to indicate the IC chip 26 instead of the metal member 16. If Applicant's assumption is incorrect, the Examiner is invited to so advise immediately.

The Examiner stated that Arai describes "a first insulating layer formed on the silicon substrate," and identified element 120 as the first insulating layer. As noted above, Arai describes element 120 of Figure 18 as a "receiving table ... composed of a plurality of dielectric layers and conductor layers layered in an alternate relationship to each other." *Col. 14, lines 52-54.* The Applicant understands that the Examiner is referring to the dielectric layers and conductor layers of the receiving table 120 as comprising "a first conductor layer formed on the first insulating layer ... ; a second insulating layer formed on the first conductive layer ... ; and a conductor layer formed on the second insulating layer." Although Arai teaches use of a plurality of dielectric and conductor layers layered in an alternate relationship, it is clear that Arai fails to

teach, and the Examiner does not point out where or how, Arai's alternate layers comprise "a first insulating layer formed on the silicon substrate", as recited in Claim 1. In other words, Arai's alternate layers may well comprise a first *conductor* layer formed on the silicon substrate. Regardless, it is clear that Arai does not teach or suggest, and the Examiner does not show where does Arai suggest, the first layer as being insulating. Moreover, Arai's alternate layers do not disclose or necessitate the precise relationship of insulating and conductor layers as recited in Claim 1. That is, Arai's does not teach or suggest "a first conductor layer formed on the first insulating layer; a second insulating layer formed on the first conductor layer; and a second conductor layer formed on the second insulating layer" as recited in Claim 1.

Furthermore, the Examiner stated the insulator 50 and the ground pattern 58 of Arai's Figure 18 as teaching a "conductor layer overlying the first insulating layer." However, as the Examiner correctly recognized, the ground pattern 58 is not "an end portion of the second conductor layer." In fact, Arai's insulator layer 50 and conductor/ground 58 do not form an end portion and have no relationship to Arai's receiving table 120. For example, layers 50 and 58 are not formed on the IC Chip 26, and do not demonstrate an overlying feature to constitute bonding portions. Thus, the Applicant submits that it would have not been obvious to one of ordinary skill in the art to recognize "an end portion of the second conductor layer overlying the first insulating layer to constitute bonding portions connected to lead wires" as recited in Claim 1.

Since Arai neither teaches nor suggests all of the claim limitations of Claim 1, Applicant respectfully submits Claim 1 for further review as patentable subject matter. Thus, the Applicant requests that the rejection of Claim 1 be withdrawn.

Consequently, because they incorporate all of the limitations of the claim from which they depend, Claims 2-10 also define patentable subject matter for at least the same reasons as set forth above with respect to the independent claim.

III. Discussion of Rejection of Claims 11-14 Under 35 U.S.C. § 103(a)

On page 6 of the Office Action, the Examiner rejected Claims 11-14 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,150,280 to Arai, et al., and further in view of U.S. Patent No. 6,384,509 to Tomonari, et al.

Because Claims 11-14 depend from Claim 1, pursuant to 35 U.S.C. § 112, ¶ 4, they incorporate by reference all the limitations of the claim to which they refer. It is therefore submitted that these claims are in condition for allowance at least for the reasons expressed with respect to the independent claim, and for their other features.

CONCLUSION

Applicant has endeavored to address all of the Examiner's concerns as expressed in the Office Action. Accordingly, arguments in support of patentability of the pending claim set are presented above. Applicant submits that the claim limitations above represent only illustrative distinctions. Hence, there may be other patentable features that distinguish the claimed invention from the prior art.

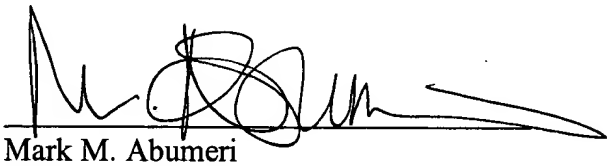
In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and, particularly, that all claims be allowed. If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully invited to call the undersigned.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 18, 2002

By: 

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